UART Assignment Report

Submitted By

**Malak Majeedullah Khan**

2021

# **UART Assignment Report**

## UART Explanation:

UART stands for Universal asynchronous receiver and transmitter. It is a devices used for short range data transmition using serial data transmission method.

The main advantage of UART is that it is low cost and more reliable that parallel data transmission sources. In UART the shift registers are used to convert the data from serial to parallel and from parallel to serial. In UART the data is transmitted as frames.

## Working of UART

As UART is an asynchronous device so it do not share the common clock. Therefore the receiver and transmitter must transmit the data at the same speed and also the same frame structure and parameter should be used. This synchronization is called is baud rate. The common baud rates are 4800, 9600, 19200, 57600, 115200.

The UART frames consist of start bit, stop bit, Data bit and parity bit. Parity bit is used for error detection while the start and stop bits tells us about the transmission and completion of the transmission.

## UART Transmitter

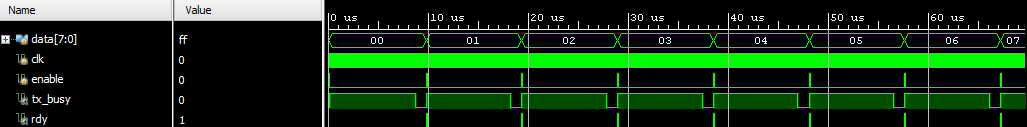
A special shift register that loads data in parallel and then shifts it out bit by bit at a specific rate. UART transmitter usually shares the baud rate generator of the UART receiver and uses an internal counter to keep track of the number of enable ticks.

## UART Receiver

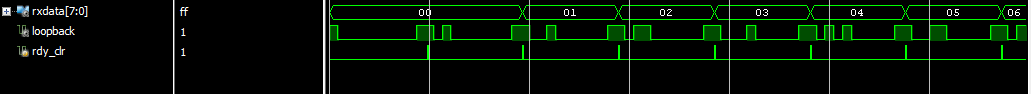
UART receiver is a shift register which shifts data bit by bit and then reassembles the data. A receiver can retrieve the data bits only by using the predetermined parameters because of no clock information obtain the data word via oversampling. An oversampling scheme basically performs the function of a clock signal. It utilizes sampling ticks to estimate the middle point of each bit.

## Results

Results for the transmitter in simulation is:



Results for the receiver in simulation is:



## References

* FPGA prototyping by Verilog examples (pong p. chu)
* <https://stackoverflow.com/questions/50142192/uart-module-and-op>
* <https://github.com/jamieiles/uart/blob/master/receiver.v>
* <https://github.com/jamieiles/uart/blob/master/transmitter.v>